Wave-Form-Generator (WFG)

Company Overview

Semify provides digital design and verification services as well as high quality IP cores for SoCs and mixed signal ASICs. The company was founded in 2021 and employs engineers with a total of 25+ years of experience in digital design for mixed signal ASICs.

IP Overview

WFG represents a flexible and scalable waveform generation solution. Due to its layered approach of separating pin control, drive, and stimuli, WFG is easily adaptable to all types of waveforms and pattern generation.

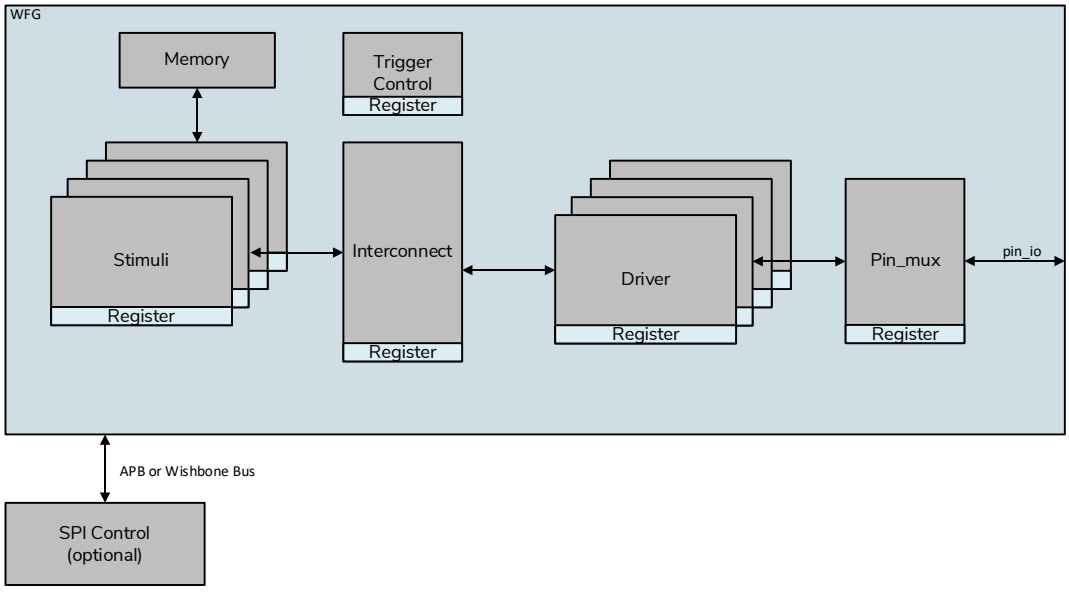
For waveform generation many different protocol drivers are supported, like SPI, I2C, UART, and I2S. In addition, it is possible to generate and record typical parallel digital patterns, supporting all common tester formats (NRZ, RO, RZ,…).

There are several different ways of generating the required stimuli. Stimuli units for generating dedicated waveforms e.g., sine wave or triangular waveform, are available. A memory-based stimuli unit allows the creation of any type of waveform or pattern.

A central sampling rate and trigger unit allows controlling the different driver units in various ways. All blocks of the WFG can be configured via an APB or Wishbone bus interface. For systems without any internal bus a SPI based command decoder is also available.

Block Diagram

The following picture shows the block diagram of the WFG.



Key Features

WFG supports many different drivers

- SPI, I2C, UART, I2S
- The number and type(s) of drivers can be configured

WFG supports a digital pattern generation driver

- Supports all common tester formats (NRZ, RO, RZ,…)
- The bit width of the pattern generation driver can be configured

WFG supports different stimuli units

- Sine wave, triangular waveform, and others
- The number of stimuli units can be configured

WGF supports a generic memory-based stimuli unit

- Supports different operating modes like looping and endless mode
- The number, the bit width and depth of the memory-based stimuli unit can be configured

WFG supports different configuration interfaces

- Standard bus interfaces APB and Wishbone
- Optional SPI based command decoder

Deliverables

- Source code
    - SystemVerilog RTL source code for the selected configuration
    - Python (cocotb) based verification environment for sanity tests
    - List of required integration tests
- Documentation
    - Datasheet
    - Integration guide
    - Configuration register description
- Setup
    - Sample FPGA project
- Support
    - Technical integration support
    - 12 month maintenance

Performance

The following table gives an overview about the used resources in an Intel Cyclone 10 LP FPGA.

Configuration	Logic Elements Embedded Multiplier	Memory	Clock frequency
Driver: ● 2 I2C ● 2 SPI ● 1 Pattern generation units (16bit) Stimuli: ● 2 Sinewave ● 2 Generic memory stimuli 2kByte each ● 2 Generic memory recorders 2kByte each SPI command decoder	4700 8	8 KB	80 MHz

Licensing

Two license options are available.

Single-Project-License: Intended for the usage of the WFG IP within a single product.
An upgrade to a Multi-Project-License is possible.

Multi-Project-License: Intended for unlimited use of the WFG IP within multiple projects.

All licenses' models are without any royalty per chip or product.

Contact

Semify e.U.

Inge-Morath-Str 64b, 8045 Graz, Austria

Email: office@semify-eda.com

Web: https://www.semify-eda.com